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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,961	02/04/2004	Arlo Aude	P05807 (11461.00.5807)	3845

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,961	AUDE, ARLO	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/04/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-13 and 16* is/are rejected.

7)☒ Claim(s) *6-7, 13-14, and 17-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/04/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities: because it is an improper dependent claim – does it depend on claim 9 instead? Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8-13, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Devecchi et al. (US 4,918,399).

Regarding claim 1, Devecchi discloses an apparatus (Fig. 6) including a multistage differential amplifier (A1, A2...) with commonly controlled input and output common mode voltages (VCMC), comprising:

first and second differential input terminals (the inverting/non-inverting inputs of A1) to convey first and second phases of a differential input signal with an associated input common mode voltage (VCMC);

first and second differential output terminals (the inverting/non-inverting output terminal of A1) to convey first and second phases of a differential output signal corresponding to said differential input signal with an associated output common mode voltage (VCMC);

a common mode control terminal (VCMC) to convey a common mode control signal for jointly controlling said input and output common mode voltages; and

a plurality of differential amplifier circuits (A1...An) successively coupled between said common mode control terminal (VCMC), said first and second differential input terminals, and said first and second differential output terminals, wherein

each one of said plurality of differential amplifier circuits (A1...An) includes first and second amplifier input terminals (the inverting/non-inverting input terminals), first and second amplifier output terminals (the inverting/non-inverting output terminals), an input control terminal (VCMC) and an output control terminal,

a first one (A1) of said plurality of differential amplifier circuits is electrically coupled to said first and second differential input terminals via said first and second amplifier input terminals (the inverting/non-inverting input terminals of A1), and is further coupled to said common mode control terminal (VCMC) via said input control terminal,

a last one (A3 or An) of said plurality of differential amplifier circuits is electrically coupled to said first and second differential output terminals via said first and second amplifier output terminals, and

said first and second amplifier input terminals and said input control terminal of each succeeding one (A2 or A3...or An) of said plurality of differential amplifier circuits is electrically coupled to said first and second amplifier output terminals (the inverting/non-inverting output terminals of A1) and said output control terminal (VCMC), respectively, of a preceding one of said plurality of differential amplifier circuits (see Fig. 6 and its text description).

Regarding claim 2, Devecchi et al. discloses the apparatus of claim 1 includes the first, second, and third circuit branches of the claimed invention (A1, A2, A3).

Regarding claim 3, Devecchi et al. discloses each of the amplifier circuits comprising a shared terminal (common sources/VCMC) via which said first, second, and third circuit branches are mutually coupled (Fig. 6).

Regarding claim 4, Devecchi et al. discloses each one of the circuit branches comprises plurality of telescopically NMOS transistors (see A2 of Fig. 6).

Regarding claims 8 & 6, Devecchi et al. discloses a multi-stage amplifier (see the abstract) with commonly controlled input and output common mode voltages (VCMC), comprising:

Input different amplifier circuitry (A1) including:

first and second input amplifier input terminals (inverting/non-inverting inputs of A1) for reception of first and second phases of a differential input signal with an associated input common mode voltage (VCMC),

first and second input amplifier output terminals,

an input amplifier control input terminal (the inverting input terminal) for reception of a common mode control signal (VCMC), and

an input amplifier control output terminal (the inverting output of A1);

intermediate differential amplifier circuitry (A2) including

first and second intermediate amplifier input terminals (the inverting/non-inverting inputs of A2) coupled to said first and second input amplifier output terminals,

first and second intermediate amplifier output terminals (the inverting/non-inverting input terminal of A2),

an intermediate amplifier control input terminal (the inverting input of A2) coupled to said input amplifier control output terminal, and

an intermediate amplifier control output terminal (the inverting output of A2); and

output differential amplifier circuitry (A3 – see lines 1-2 of the abstract) including

first and second output amplifier input terminals (the inverting/non-inverting inputs of A3) coupled to said first and second intermediate amplifier output terminals,

first and second output amplifier output terminals for conveyance of first and second phases of a differential output signal corresponding to said differential input signal with an associated output common mode voltage corresponding to said input common mode voltage,

an output amplifier control input terminal (the inverting input terminal of A3 or An – the last/output stage) coupled to said intermediate amplifier control output terminal, and an output amplifier control output terminal (Fig. 6).

Regarding claim 9, Devecchi et al. discloses the apparatus of claim 8 includes the first, second, and third circuit branches of the claimed invention (A1, A2, A3).

Regarding claim 10, Devecchi et al. discloses each of the amplifier circuits comprising a shared terminal (common sources/VCMC) via which said first, second, and third circuit branches are mutually coupled (Fig. 6).

Regarding claim 11, Devecchi et al. discloses each one of the circuit branches comprises plurality of telescopically NMOS/CMOS transistors (see A2 of Fig. 6).

Prior Art

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (see cited references on PTO-892 Form accompanied with this Office Action).

Allowable subject matter

4. Claims 6-7, 14-15, and 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN
May 26, 2005

PEGUY JEANPIERRE
PRIMARY EXAMINER